Amendments to the Specification

Please amend the paragraph under the "Related Patent Data" section on page 1 to read as follows:

B1

This patent resulted from a divisional application of U.S. Patent Application Serial No. 09/843,116, filed on April 24, 2001, and which is now U.S. Patent No. 6,458,699 B1. The application which became U.S. Patent No. 6,458,699 B1 resulted from a divisional application of U.S. Patent Application Serial No. 09/429,236, filed on October 28, 1999, and which is now U.S. Patent No. 6,509,239 B1. The application which became U.S. Patent No. 6,509,239 B1 resulted from a divisional application of U.S. Patent Application Serial No. 09/023,239, filed on February 13, 1998, and which is now U.S. Patent No. 6,159,852.

Please amend the first paragraph in the "Background of the Invention" section, beginning on line 11 of page 1, as follows:

Device geometry continues to shrink in semiconductor circuitry fabrication. For example, field effect transistor gate width is now commonly below one micron and source/drain junction depth 1000 Angstroms or less. A challenge in such constructions is to reduce parasitic source/drain serial resistance while maintaining low source/drain diode leakage. Such resistance can be reduced by providing a thicker ~~salicide~~ silicide over the source/drain. Such is typically provided by depositing a metal layer on the source/drain which typically comprises monocrystalline silicon. A subsequent anneal causes a reaction which consumes a portion of the silicon to form the silicide. However, large consumption of silicon to form the desired thicker ~~salicide~~ silicide results in the ~~salicide/junction~~ silicide/junction interface being very close to the base of the junction. This causes source/drain diode leakage current to the substrate to increase.

Please add the following paragraph starting at line 17 on page 6:

B3

Fig. 16 is an alternate view of that depicted by Fig. 15.

Please amend the paragraph beginning at line 10 on page 10 as follows:

B4

Alternate exposed crystalline surfaces, by way of example only, utilizable in the context of the invention include silicides (such as $TiSi_x$ and Wsi_4), crystalline dielectrics (such as barium strontium titanate and Ta_2O_5), aluminum, copper, aluminum-copper alloys, tungsten, and other crystalline metals or metal-like materials. Selectivity in the ~~deposition in~~ deposition is expected to be greatest where the reactor atmosphere during the time period of deposition is substantially void of a gas comprising a conductivity enhancing dopant, or other gases, although conductivity enhancing gases (such as B_2H_6) are expected to provide functional selectivity in accordance with the invention.

Please amend the paragraph beginning at line 6 on page 16 as follows:

Referring to Fig. 15, a capacitor dielectric layer 89 is deposited followed by deposition of a second capacitor electrode layer 90 to form a capacitor 93. Such can be formed by conventional or other processing. For example, techniques of the invention as described above can be utilized to selectively deposit second capacitor electrode layer 90 on dielectric layer 89 where such is fabricated to be crystalline. For example, barium strontium titanate and Ta_2O_5 are exemplary crystalline capacitor dielectric layer materials. Such material can be deposited over first capacitor electrode 88, patterned if desired to provide exposed amorphous material and the crystalline material 89 where desired, and a selective deposition (Fig. 16) as described above then conducted.

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